Hybrid PWM technology of cascaded H-bridge multilevel active rectifier

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Abstract: This paper presents a control strategy for the cascaded H-bridge rectifier (CHBR). Using PI based voltage controller and proportional-resonant (PR) current controller, and adding low frequency (step modulation) and high frequency (pulse width modulation) mixed modulation control algorithm, the control objectives of shaping input AC current, correcting power factor and stabilizing DC side voltage are realized. By building a seven level CHBR simulation model based on MATLAB / Simulink, the feasibility and effectiveness of the control strategy are verified by simulation.

1. Introduction

In recent years, with the development of power electronic technology and modern control theory, the application of power electronic devices in the field of high voltage and high power is increasing. Limited by the withstand voltage conditions of the device, the research on multilevel topology and related control theory has received extensive attention. Multilevel (ML) converter has become the most suitable choice in high power applications. Many multilevel converter structures have been covered in previous literature, including neutral point clamped (NPC) / active NPC, cascaded H-bridge (CHB) converter, flying capacitor (FC) and many other improvements. Among them, CHB converter has attracted more attention due to its high modularity, less use of electronic components and uniform distribution of semiconductor losses among the power switches [1]. It has been widely used in the fields of high-voltage and high-power motor drive, power electronic transformer, active filter and reactive power compensation [2] - [6].

As a typical application of CHB structure, cascaded H-bridge rectifier (CHBR) also has many characteristics of this topology. Controlling the DC voltage balance of all levels of power units is the premise to ensure the safe and reliable operation of the whole CHBR system, and is the basis for the application of low-voltage power devices in high-voltage situations. Therefore, it is very important to study the strategy of maintaining DC side voltage stability and regulating AC side input current quickly and accurately.

Different DC side voltage balancing control algorithms are proposed in [7] - [12]. A control scheme based on low frequency step modulation is adopted in [7]. This strategy controls the DC side voltage balance by looking up the table to select the switch redundancy state. A passive control strategy considering energy balance is introduced in [8]. The strategy decouples the CHBR to realize the energy control of all levels of H-bridge units, so as to realize the control of DC side voltage at all levels. In the control, a passive controller is designed to decouple the H-bridge completely. A balance strategy based on carrier phase-shift modulation technology is proposed in [9], [10]. The power balance between modules at all levels is realized by adjusting the phase and amplitude of modulation voltage at all levels. In [11], a control scheme based on PI controller is proposed to alleviate the voltage imbalance of cascaded H-bridge by controlling the power flow of the converter. In [12], a stable voltage balance method is proposed, which uses the estimated DC-link capacitor energy to track the DC voltage changes of the converter based on an adaptive resonance algorithm.

Although the above control algorithms are effective, there are still some disadvantages such as current spectrum and variable switching frequency uncertainty, sensitivity to system model accuracy, complex parameter design and heavy calculation workload [13].

In [14], CHBR voltage balancing technology with hybrid modulation strategy is proposed, which takes advantage of low frequency switching and high frequency pulse width modulation technology. A low frequency control loop is added to manage the working state of each cell to realize the voltage balance between the H-bridge cells in [15]. However, the system also has the influence of variable switching frequency. Therefore, in this paper, an improved hybrid PWM technology is proposed to adjust the input AC current and stabilize the DC capacitor voltage.

2. System configuration

2.1 Rectifier structure

As shown in Fig. 1, the CHBR consists of three H-bridge modules in series. Each H-bridge module consists of four power semiconductor devices and a DC side capacitor. v_s represents the input AC voltage source at the grid side, i_{in} represents the input AC current at the grid side, L_f represents the filter inductance at the grid side; the steady-state value of DC side voltage of each power unit is expressed as $V_{dc1}, V_{dc2}, V_{dc3}$; $I_{dc1}, I_{dc2}, I_{dc3}$ is the output current of each stage; R_{L1}, R_{L2}, R_{L3} is the resistance which is used to equivalent DC side load.
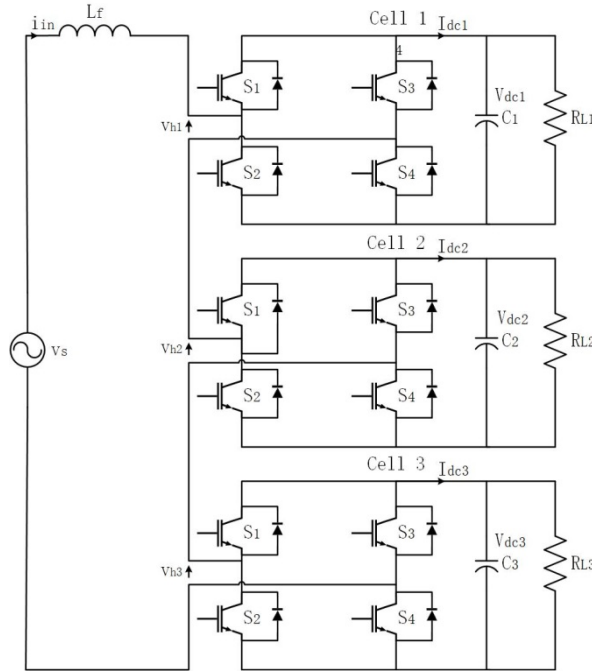

Fig. 1 Cascaded H bridge rectifier with three modules.

2.2 controller configuration

The proposed control scheme is shown in Fig. 2. The controller should determine the control mode from h_1 to h_3 to achieve the control goals of adjusting input current, correcting power factor and stabilizing DC side voltage [15]. In this paper, a two-stage cascade controller is used to achieve the control goal. The outer loop is tracked by a voltage controller based on PI, which adjusts the total DC voltage from $\sum_{i=1}^{3} V_{dci}$ to $N \times V_{dc}^*$. The output of PI controller is the reference current to control the amplitude of AC current. The phase-locked loop is used to generate the input current which is synchronized with the phase and frequency of the grid voltage. The inner loop is a current controller. It is well known that the PR controller has a good ability to track AC signals and can provide infinite gain at ω [13]. Because it is easy to implement and can realize zero steady-state

error of phase and amplitude, this paper uses PR controller [16]. The output v_r of PR controller is used as the reference voltage of AC side.
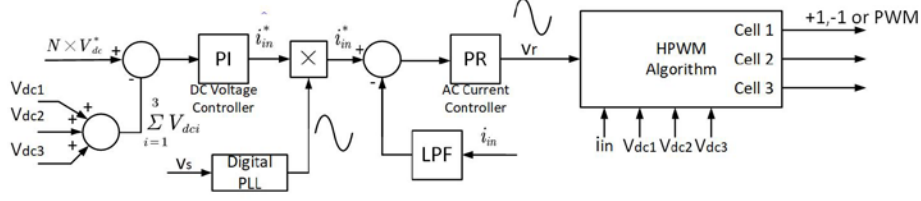

Fig. 2 The controller block diagram of the cascaded H-bridge.

The switch function $h_i(i=1,2,3)$ has four operation modes: " +1", " -1", "0" and PWM [15]. In each switching cycle, the balance algorithm applies the appropriate switching mode for each power unit by comparing v_r. When $h_i=+1$, S_1 and S_4 are on, the AC side output voltage of the module is $+V_{dci}$; when $h_i=-1$, S_2 and S_3 are on, the AC side output voltage of the module is $-V_{dci}$; when $h_i=0$, S_2, S_4 (or S_1, S_3) is on, and the AC side output voltage of the module is 0. The switching function h_i and its corresponding output AC voltage are shown below.

$$v_{hi}=\begin{cases} +V_{dci} & h_i=+1 \\ -V_{dci} & h_i=-1 \\ 0 & h_i=0 \\ PWM\ Reference & h_i=PWM \end{cases} \quad (i=1,2,3) \tag{1}$$

3. proposed modulation strategy

The main challenges associated with the CHBR control are: 1) adjusting the input current and controlling the input power factor; 2) maintaining voltage balance across DC side capacitors [15]. The first goal will be achieved through the main function of the switching strategy. The second goal means adjusting the DC voltage of each unit to a reference value V_{dc}^*. If the H-bridge modules are the same and the power distribution is equal, a symmetrical switching strategy similar to PS-PWM can be used. However, in the case of unbalanced load and uneven power distribution, more complex modulation strategies must be used.

In order to make full use of low frequency (step modulation) and high frequency (PWM) modulation techniques, a hybrid modulation method is adopted [15]. The specific steps of the proposed control algorithm are as follows:

Define the voltage area. v_r is in the Kth voltage region if:

$$\sum_{i=1}^{K-1} V_i < |v_r| < \sum_{i=1}^{K} V_i + V_K \tag{2}$$

Where $V_1 - V_N$ represents the DC side voltage of each power unit $V_{dc1} - V_{dcN}$ in ascending order.

(2) Assign appropriate operation modes to different units according to the control rules shown in Fig. 3 after the voltage region of v_r and the positive and negative of i_{in} and v_r are determined.

$V_1, V_2, \cdots V_N$ are the DC side voltage in ascending order, i.e. $V_1 < V_2 < \cdots < V_N$. In each switching cycle, only one unit works in PWM mode, and the others are in "+ 1" or "- 1" mode.

According to the block diagram, we can get that if $v_r > 0, i_{in} > 0$, and $N-K$ is even, then the units corresponding to $V_1, V_2, \cdots, V_{\frac{N+K}{2}-1}$ are set to "+ 1" mode, unit corresponding to $V_{\frac{N+K}{2}}$ is in

PWM mode, and units corresponding to $V_{\frac{N+K}{2}+1}, \cdots, V_{N-1}, V_N$ are in "- 1" mode. The operation is similar in other states.
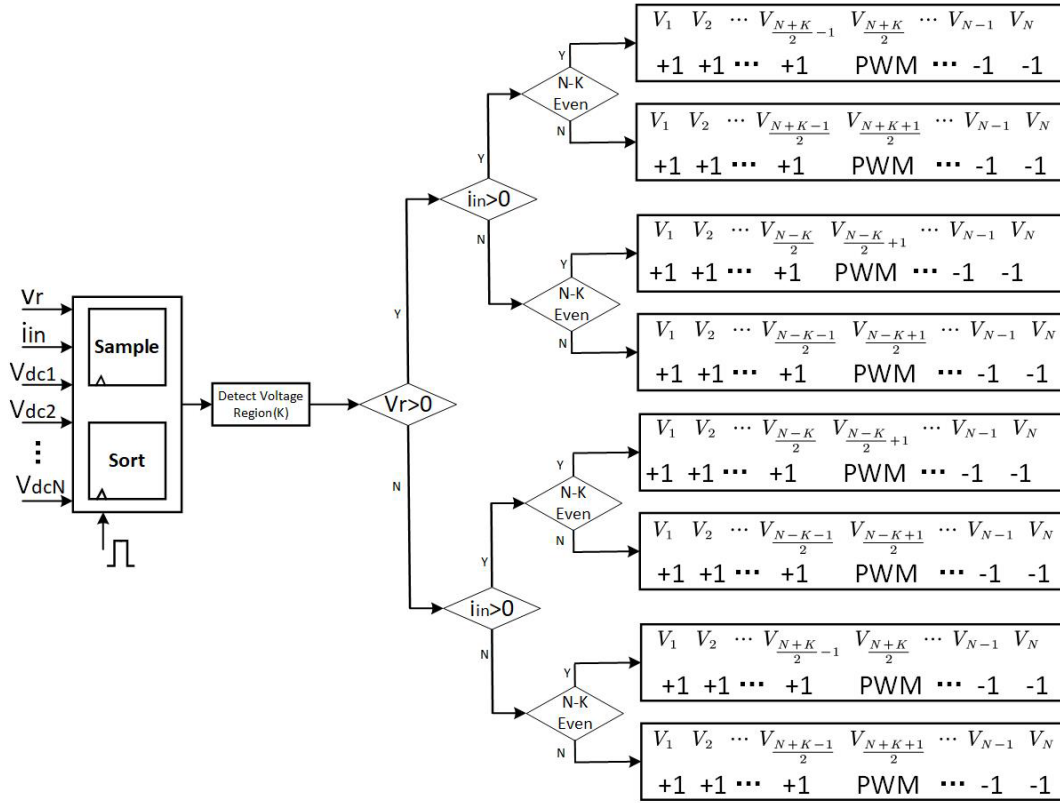

Fig. 3 Flow chart of control algorithm.

Therefore, the proposed modulation strategy uses a combination of high-frequency and low-frequency switches, which can significantly reduce the switching loss. The low-frequency switch is responsible for assigning the optimal switching state for each unit to maintain the balance of capacitor voltage, while the high-frequency SPWM is used to shape the grid current [16]. Assuming that the i th unit works in PWM mode, the reference voltage of PWM module $v_{r,PWM}$ is derived as follows:

$$V_{r,PWM} = V_r - \sum_{j=1, j \neq i}^{N} h_j V_{dcj} \qquad (3)$$

In other words, the reference voltage of the i th unit shall be determined such that the resultant total AC voltage is equal to v_r. The modulation signal $v_{r,PWM}$ is obtained by the difference between v_r and V_{dci}, and is compared with the triangular carrier in order to generate the switch command of the i th unit and control the on-off of the semiconductor device [16].

4. Simulation results and analysis

In order to test the effectiveness of the control strategy, based on the above theoretical analysis, the CHBR model of three power units is built in MATLAB / Simulink and verified by simulation. The parameter settings are shown in Table 1, and the simulation results are shown in Fig. 4 through Fig. 9.

Table 1 System simulation parameters

Parameter	Value
Number of H-bridges	3
Input AC Voltage	120V
Input Filter Inductor	8mH
DC Link Voltage of Cells	80V
DC Link Capacitors of Cells	6mF
Cell Load Resistance	50Ω
Rated Cell Output Power	128W
Input Grid Frequency	50Hz
Low Frequency Switching	250Hz
High Frequency Switching	2500Hz

Fig. 4 shows that under the condition of rated parameters and balanced load, the grid side voltage and current of CHBR are balanced and the phase is consistent. The frequency spectrum of AC terminal voltage, grid current and DC load voltage is obtained by using the fast Fourier transform analysis toolbox of MATLAB / Simulink. As shown in Fig. 5, THD of AC terminal voltage is 25.59%; THD of grid current is 1.51%, and harmonics with frequency of 50 Hz integer times account for a large proportion; THD of DC load voltage is 0.53%.
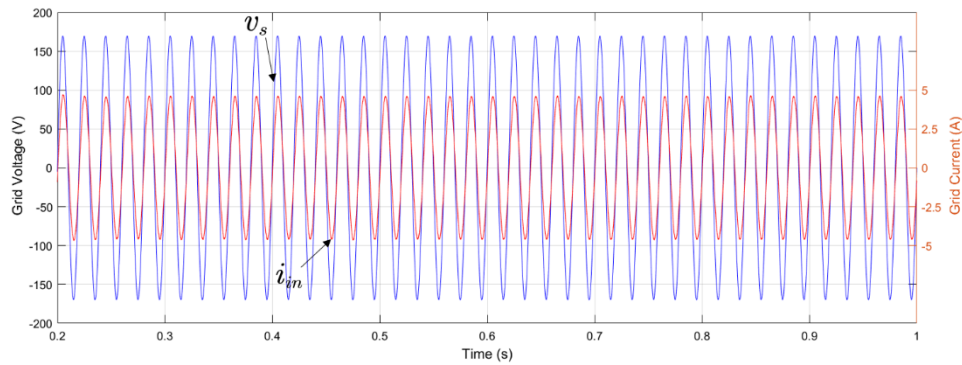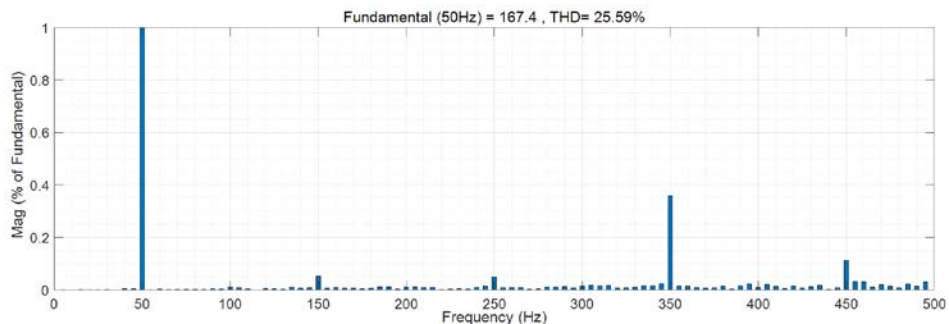

Fig. 4 simulation results of the system under rated conditions
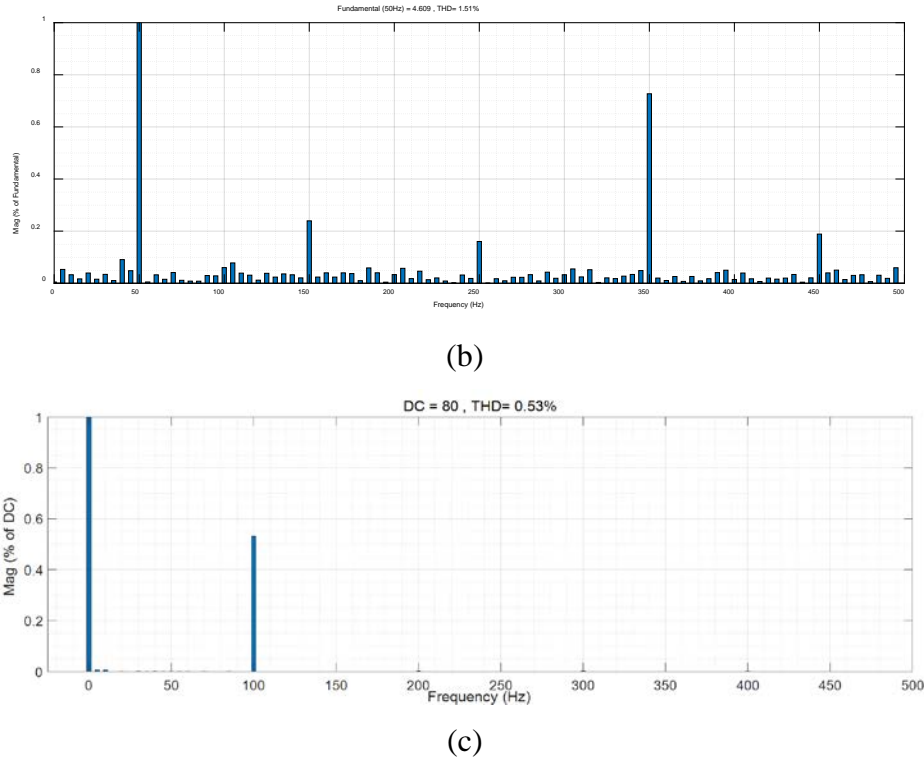

(a)

Fundamental (50Hz) = 4.609 , THD= 1.51%

(b)

DC = 80 , THD= 0.53%

(c)

Fig. 5 The frequency spectrum of (a) AC terminal voltage, (b)grid current, and (c) DC load voltage.

Fig. 6 and Fig. 7 verify the dynamic performance of the system. First of all, Fig. 6 shows the corresponding change of DC side capacitor voltage under the condition of 30% grid side voltage disturbance at 0.5s. It can be seen from the figure that before the disturbance, the control system stabilizes the DC voltage near the rated value of 80V. After the disturbance, the system successfully compensates the disturbance on the grid side and maintains the voltage balance between DC capacitors. Then, Fig. 7 shows the waveform of DC side voltage and grid side input current when $R_{L1} = 50\Omega, R_{L2} = 70\Omega, R_{L3} = 50\Omega$ for 0.5s. It can be seen from the figure that when the load changes, the voltage of the DC side capacitor is disturbed. However, the control system quickly responds to the load disturbance and adjusts the DC voltage to the required reference value. Therefore, the control algorithm has small steady-state error and good dynamic performance, and can stabilizing DC side voltage well under various conditions.
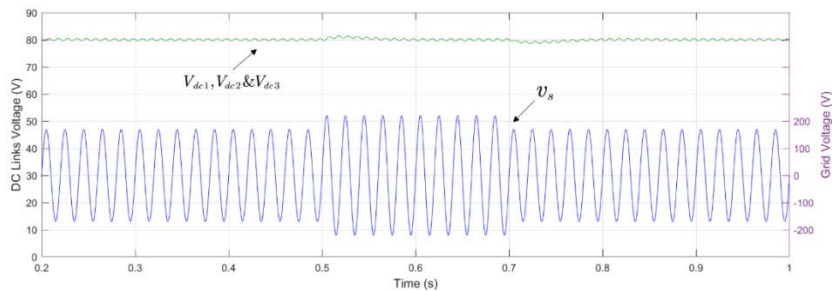

Fig. 6 Simulation results of the system under grid side voltage disturbances (30%).
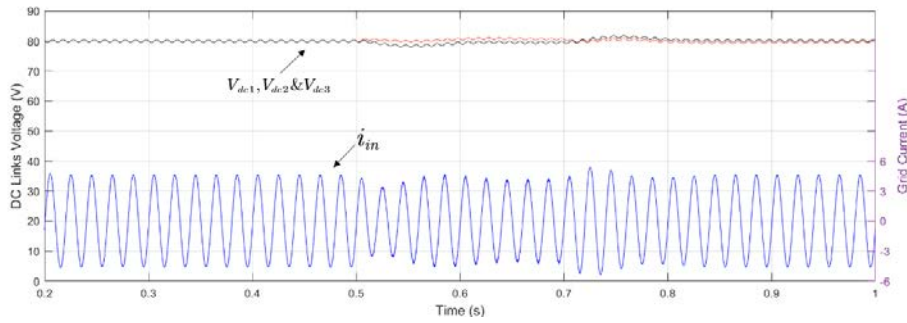
Fig. 7 Simulation results of the system under unbalanced load conditions.

5. Conclusion

Aiming at the important problems of how to adjust the AC side input current of CHBR and keep the DC side voltage balance at all levels, a control strategy using hybrid modulation method is proposed in this paper. The strategy can adjust the input current to sinusoidal form and stabilize the DC voltage. The simulation results show that the proposed control scheme can eliminate the steady-state error and improve the dynamic performance of the system, which verifies the accuracy and feasibility of the theoretical analysis and control algorithm, and has a broad application prospect in high-voltage and high-power CHBR.

References

[1] A. Moeini, H. Iman-Eini and A. Marzoughi, "DC link voltage balancing approach for cascaded H-bridge active rectifier based on selective harmonic elimination-pulse width modulation," in IET Power Electronics, vol. 8, no. 4, pp. 583-590, 4 2015, doi: 10.1049/iet-pel.2014.0086.

[2] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," in IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2930-2945, Dec. 2007, doi: 10.1109/TIE.2007.907044.

[3] T. Zhao, G. Wang, S. Bhattacharya and A. Q. Huang, "Voltage and Power Balance Control for a Cascaded H-Bridge Converter-Based Solid-State Transformer," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1523-1532, April 2013, doi: 10.1109/TPEL.2012.2216549.

[4] W. Jiang, L. Huang, L. Zhang, H. Zhao, L. Wang and W. Chen, "Control of Active Power Exchange With Auxiliary Power Loop in a Single-Phase Cascaded Multilevel Converter-Based Energy Storage System," in IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 1518-1532, Feb. 2017, doi: 10.1109/TPEL.2016.2543751.

[5] C. Wang, Y. Zhuang, J. Jiao, H. Zhang, C. Wang and H. Cheng, "Topologies and Control Strategies of Cascaded Bridgeless Multilevel Rectifiers," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 432-444, March 2017, doi: 10.1109/JESTPE.2016.2626788.

[6] C. Cecati, A. Dell'Aquila, M. Liserre and V. G. Monopoli, "Design of H-bridge multilevel active rectifier for traction systems," in IEEE Transactions on Industry Applications, vol. 39, no. 5, pp. 1541-1550, Sept.-Oct. 2003, doi: 10.1109/TIA.2003.816515.

[7] C. Cecati, A. Dell'Aquila, M. Liserre and V. G. Monopoli, "A passivity-based multilevel active rectifier with adaptive compensation for traction applications," in IEEE Transactions on Industry Applications, vol. 39, no. 5, pp. 1404-1413, Sept.-Oct. 2003, doi: 10.1109/TIA.2003.816552.

[8] A. Dell'Aquila, M. Liserre, V. G. Monopoli and P. Rotondo, "An energy-based control for an n-H-bridges multilevel active rectifier," in IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 670-678, June 2005, doi: 10.1109/TIE.2005.843971.

[9] J. A. Barrena, L. Marroyo, M. Á. Rodriguez Vidal and J. R. Torrealday Apraiz, "Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM," in IEEE Transactions on Industrial Electronics, vol. 55, no. 1, pp. 21-29, Jan. 2008, doi: 10.1109/TIE.2007.906127.

[10] X. She, A. Q. Huang and G. Wang, "3-D Space Modulation With Voltage Balancing Capability for a Cascaded Seven-Level Converter in a Solid-State Transformer," in IEEE Transactions on Power Electronics, vol. 26, no. 12, pp. 3778-3789, Dec. 2011, doi: 10.1109/TPEL.2011.2142422.

[11] T. Xinghua, L. Yongdong and S. Min, "A Pi-based control scheme for primary cascaded H-bridge rectifier in transformerless traction converters," 2010 International Conference on Electrical Machines and Systems, Incheon, 2010, pp. 824-828.

[12] V. Blahnik, T. Kosan, Z. Peroutka and J. Talla, "Control of a Single-Phase Cascaded H-Bridge Active Rectifier Under Unbalanced Load," in IEEE Transactions on Power Electronics, vol. 33, no. 6, pp. 5519-5527, June 2018, doi: 10.1109/TPEL.2017.2748218.

[13] G. Jean-Pierre, N. Altin, A. E. Shafei and A. Nasiri, "A Control Scheme Based on Lyapunov Function for Cascaded H-Bridge Multilevel Active Rectifiers," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 2021-2026, doi: 10.1109/APEC39645.2020.9124234.

[14] M. Moosavi, G. Farivar, H. Iman-Eini and S. M. Shekarabi, "A voltage balancing strategy with extended operating region for cascaded H-bridge converters," in IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 5044-5053, Sept. 2014, doi: 10.1109/TPEL.2013.2286270.

[15] H. Iman-Eini, J. Schanen, S. Farhangi and J. Roudet, "A Modular Strategy for Control and Voltage Balancing of Cascaded H-Bridge Rectifiers," in IEEE Transactions on Power Electronics, vol. 23, no. 5, pp. 2428-2442, Sept. 2008, doi: 10.1109/TPEL.2008.2002055.

[16] M. Moosavi, G. Farivar, H. Iman-Eini and S. M. Shekarabi, "A voltage balancing strategy with extended operating region for cascaded H-bridge converters," in IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 5044-5053, Sept. 2014, doi: 10.1109/TPEL.2013.2286270.